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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,034	12/11/2003	Kunal N. Taravade	01-916/1D	8429

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LSI LOGIC CORPORATION  
1621 BARBER LANE  
MS: D-106  
MILPITAS, CA 95035

EXAMINER

GEORGE, PATRICIA ANN

ART UNIT	PAPER NUMBER
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1765

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/733,034

Applicant(s)

TARAVADE ET AL.

Examiner

Patricia A. George

Art Unit

1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 11 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 12-16 is/are pending in the application.
- 4a) Of the above claim(s) 16 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 12-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☒ Claim(s) 12-16 are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Response to Amendment*

Amendment to claims have been received and by this amendment, claims 1-11 have been canceled.

### *Election/Restrictions*

This application contains claims directed to the following patentably distinct species of the claimed invention:

**Species A:** capacitor in the form of a plate

**Species B:** capacitor in the form of cylindrical

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, claim 12 is generic.

Applicant is advised that a reply to this requirement must include an identification of the species that is elected consonant with this requirement, and a listing of all claims readable thereon, including any claims subsequently added. An argument that a claim is allowable or that all claims are generic is considered nonresponsive unless accompanied by an election.

Upon the allowance of a generic claim, applicant will be entitled to consideration of claims to additional species which are written in dependent form or otherwise include all the limitations of an allowed generic claim as provided by 37 CFR 1.141. If claims are added after the election, applicant must indicate which are readable upon the elected species. MPEP § 809.02(a).

Should applicant traverse on the ground that the species are not patentably distinct, applicant should submit evidence or identify such evidence now of record showing the species to be obvious variants or clearly admit on the record that this is the case. In either instance, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) of the other invention.

During a telephone conversation with Howard Moore on 07 September 2005 a provisional election was made with traverse to prosecute the invention of Species A: capacitor in the form of a plate, claims 12- 15. Affirmation of this election must be made by applicant in replying to this Office action. Claim 16 is withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected species.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

### ***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 12, 13, 14, and 15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 2, 7 and 4 of U.S. Patent No. 6,699,766.

Claim 1 of U.S. Patent No. 6,699,766 teaches a method of fabricating a capacitor on a substrate, including steps of: performing capacitor foundation formation on the substrate', depositing polish stop layer material on the capacitor foundation and the substrate', etching a first capacitor electrode region on the capacitor foundation formation and a transistor gate region on the substrate; depositing a first conductive material in the etched first capacitor electrode region and the transistor gate region', performing chemical mechanical polishing on the deposited first conductive material to yield a gate electrode and a first capacitor electrode, depositing a dielectric material over the gate electrode and the first capacitor electrode', etching a second capacitor electrode region in the dielectric material over the first capacitor electrode and into the

first capacitor electrode material', forming a capacitor dielectric layer over the first capacitor electrode', depositing a second conductive material in the etched second capacitor electrode region; and performing chemical mechanical polishing on the deposited second conductive material to yield a second capacitor electrode.

Claim 1 of U.S. Patent No. 6,699,766 does not teach the deposition of a polish stop layer material on the capacitor foundation and the substrate, as in claim 12.

Claim 2 of U.S. Patent No. 6,699,766 illustrates it is expectable and conventional to include the capacitor foundation includes an oxide layer, utilized as a CMP as a polish stop.

Differences are noted between applicants' claims and claim 2 of U.S. Patent No. 6,699,766. Applicants' claims do not require the polish stop layer to be formed of a conventional material, such as oxide, as in claim 2, of U.S. Patent No. 6,699,766. In addition, applicants' claims are silent about "a transistor gate region" being the same as "a gate electrode region" as defined by claim 1, of U.S. Patent No. 6,699,766.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the use of oxide as the polish stop layer, as claimed in US Patent 6,699,766 illustrates it is a conventionally used material. Further, It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a gate electrode region, of US Patent 6,699,766, is the same area as a transistor gate region, of applicants claim 12, because the term "gate electrode regions" encompasses a "transistor gate region". Nothing unexpected occurs by modifying the use of the gate terminology or using oxide as the stop layer.

As to claim 13, see discussion above for the polish stop layer material on the capacitor foundation substrate comprising an oxide.

As to claim 14, claim 7 of U.S. Patent No. 6,699,766 illustrates use of a polish stop layer material comprising a nitride.

As to claim 15, claim 4 of U.S. Patent No. 6,699,766 illustrates first and second electrodes to be in the form of a plate.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

  
PAG  
09/05

Patricia A George  
Examiner  
Art Unit 1765

  
NADINE G. NORTON  
SUPERVISORY PATENT EXAMINER